Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT

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***Abstract*—This paper presents the development of a simulation model for high-voltage gallium nitride (GaN) high-electron-mobility transistors (HEMT) in a cascode structure. A method is proposed to accurately extract the device package parasitic inductance, which is of vital importance to better predict the high-frequency switching performance of the device. The simulation model is verified by a double-pulse tester, and the results match well both in terms of device switching waveform and switching energy. Based on the simulation model, an investigation of the package influence on the cascode GaN HEMT is presented, and several critical parasitic inductances are identified and verified. Finally, a detailed loss breakdown is made for a buck converter, including a comparison between hard switching and soft switching. The results indicate that the switching loss is a dominant part of the total loss under hard-switching conditions in megahertz high-frequency range and below 8∼10 A operation current; therefore, soft switching is preferred to achieve high-frequency and high-efficiency operation of the high-voltage GaN HEMT.**

***Index Terms*—Cascode structure, gallium nitride (GaN) high-electron-mobility transistors (HEMT), parasitic inductance, simulation model, soft switching.**

I. Introduction

ADVANCED power semiconductor devices have consistently proven to be a major force in pushing the progressive development of the power conversion technology. The emerging gallium nitride (GaN)-based power semiconductor device is considered a promising candidate to achieve high-frequency, high-efficiency, and high-power-density power conversion [1]–[17]. Due to the advantages of the material, the GaN high-electron-mobility transistors (HEMT) has the features of a wide bandgap, high electron mobility, and high electron velocity [1], [2]. Thus, a better figure of merit can be projected for the GaN HEMT [3] than for the state-of-the-art Si MOSFETs, which allows the GaN HEMT to switch with faster transition and lower switching loss. By using the GaN HEMT in a circuit design, the switching frequency can be pushed up to megahertz frequencies, and continue to have high efficiency [4]–[11].

To evaluate the switching performance of the GaN HEMT, this paper uses a device simulation model. Device manufacturers often have physics-based device models. These models can reveal detailed characteristics of the device [18], but the simulation is very time consuming [19]. As a supplement, a behavior-level simulation model is necessary. For the Si MOSFET, such behavior-level simulation model is mature [20], while only a few works can be found about the emerging SiC- or GaN-based devices, and most of them are based on a Si device model with specific modifications [21]–[23].

Depending on its physical structure, the GaN transistor can be categorized as working in either enhancement mode or in depletion mode. So far, the application of the enhancement-mode (E-mode) GaN transistor is limited due to critical driving issues as addressed in [5], [6], and [12]. The E-mode GaN transistor is fully enhanced with a gate-to-source voltage between 4.5 to 5 V, and will fail if the gate-to-source voltage exceeds 6 V. So the margin to ensure safe operation is very small. On the contrary, the depletion-mode GaN transistor is preferred due to simple and safe gate drive. To use a high-voltage depletion-mode GaN transistor in a circuit design, a low-voltage Si MOSFET is used in series to drive the high-voltage GaN transistor, which is well-known as a cascode structure. The study in this paper is based on the 600-V cascode GaN HEMT in TO-220 package developed by Transphorm Inc. A corresponding preliminary GaN HEMT simulation model is also provided by Transphorm Inc. The model is verified to have good characteristics in most aspects, but it fails to accurately predict package parasitic inductance. However, the package parasitic inductance is of vital importance due to the cascode structure and the high switching frequency.

This paper first introduces the process to accurately extract the package parasitic inductance of a cascode GaN HEMT, including both self-inductance and mutual-inductance. Next, the accuracy of the simulation model is verified by experiment. A double-pulse tester (DPT) is carefully designed and built as the test circuit with minimized parasitics to reveal the intrinsic switching performance of the device. Based on the simulation mode, an investigation of package influence on device switching performance is made, which reveals several critical parasitic inductances that have major impacts on the device switching performance. Finally, a detailed loss breakdown and analysis are made based on a buck converter, illustrating that soft-switching

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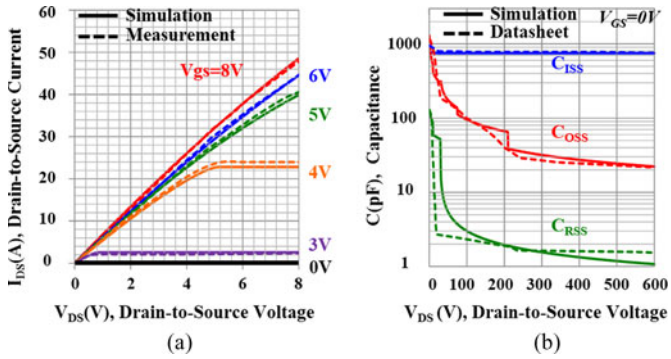

Fig. 1. (a) *I–V* characteristic and (b) *C–V* characteristic comparison between simulation and measurement/datasheet.

techniques are preferred for megahertz high-frequency and high-efficiency operation of the cascode GaN HEMT.

II. Package Parasitic Inductance Extraction

For the cascode GaN HEMT studied in this paper, a SPICE-based behavior-level simulation model is initially provided by the device manufacturer Transphorm Inc. SIMetrix is used for conducting the circuit simulation. The device's primary characteristics, like the *I–V* characteristic and the *C–V* characteristic, are simulated and verified by matching measurements or datasheets (as shown in Fig. 1). The *I–V* curves under different gate-source voltages are measured by a Tektronix 371B programmable high-voltage curve tracer.

The original simulation model lacks accurate package parasitic inductance, which is of major importance to describe the dynamic characteristic of the device. Fig. 2 shows the bonding diagram of the cascode GaN HEMT in a traditional TO-220 package and its corresponding schematic. The figure clearly indicates that many parasitic inductances are introduced due to the interconnections between the GaN die and the Si die, and between the dies and the lead frame. Moreover, as the currents with fast transitions are confined in such a small area, the coupling effects between different conductors are significant. The coupling coefficients of Lint1 with the other inductances are labeled in Fig. 2(b).

In this paper, the extraction of package parasitic inductance is implemented by Ansoft Q3D Extractor finite-element analysis (FEA) simulation. According to the electromagnetic theory, many parameters, like the dimensions, the positions, and the current directions of the conductors, have a significant effect on self-inductance and mutual-inductance. Among these factors, the dimensions and positions of the conductors can be easily determined based on the device bonding diagram. However, the current directions are sensitive and important, but difficult to define correctly, which will determine the polarity of coupling coefficient and thus have a significant impact. For devices working in switch mode, it is critical to verify the current paths and differentiate parasitic inductance under turn-on and turn-off conditions. However, such criteria are often neglected.

To be specific, Fig. 3 shows a cascode GaN HEMT that is assumed to be working as an active switch in a switch-mode power supply. The blue loop, the red loop, and the green loop

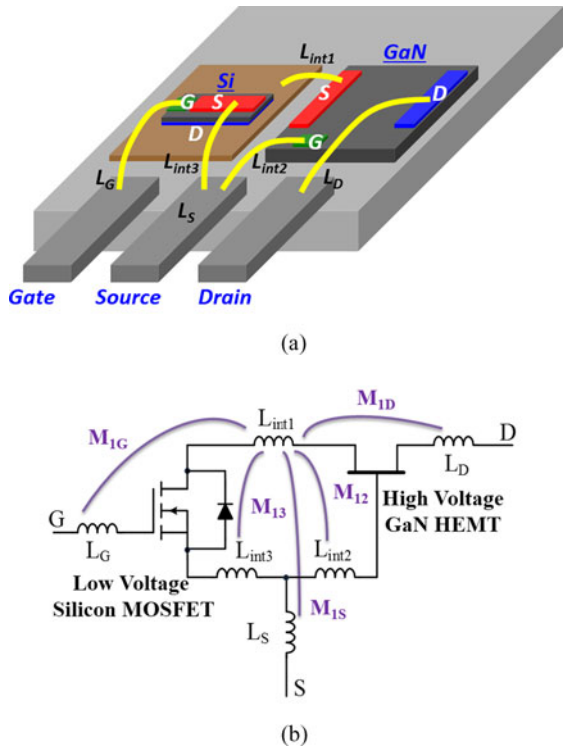

Fig. 2. Cascode GaN HEMT (a) TO-220 package simplified bonding diagram and (b) TO-220 package parasitic inductance schematic.

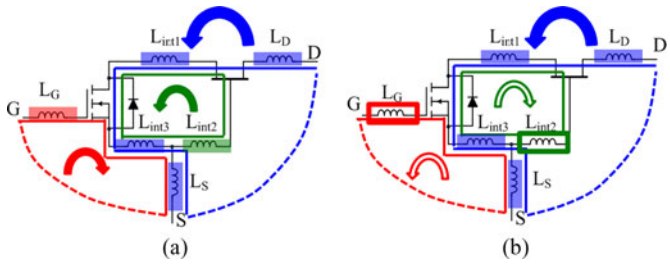

Fig. 3. Current directions in the cascode structure during (a) turn-on transition and (b) turn-off transition.

represent device's power loop, Si MOSFET driving loop, and GaN HEMT driving loop, respectively. The arrows indicate the current directions of each loop. During turn-on and turn-off transitions, the power loop maintains its direction; the two driving loops will change their directions instead. Another important assumption is that when a conductor involves in more than one loop, the specified current direction will follow the current direction in a power loop. According to these criteria, the current direction of each conductor can be determined. The inductances can then be accurately extracted by solving Maxwell equations in the FEA simulation, which are shown in Table I. Different values are applied when conducting simulation.

III. Simulation Model Verification in the DPT

A. Modeling of the DPT

In order to verify the accuracy of GaN HEMT simulation model, a DPT is carefully designed and built with minimized

TABLE I
PACKAGE PARASITIC INDUCTANCE EXTRACTED BY ANSOFT Q3D FEA SIMULATION

	Turn-on	Turn-off
L_{int1}	0.27 nH	0.26 nH
L_{int2}	0.23 nH	0.17 nH
L_{int3}	0.24 nH	0.43 nH
L_S	0.57 nH	0.89 nH
L_G	2.87 nH	3.12 nH
L_D	1.89 nH	1.62 nH

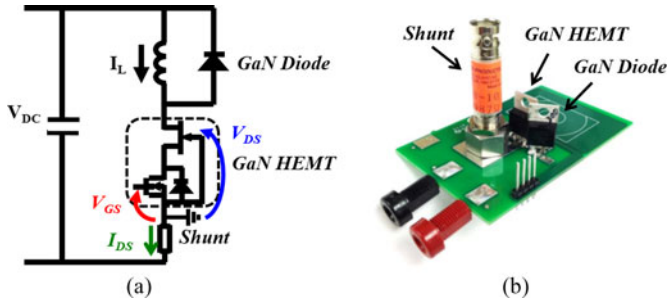

Fig. 4. DPT (a) schematic and (b) prototype.

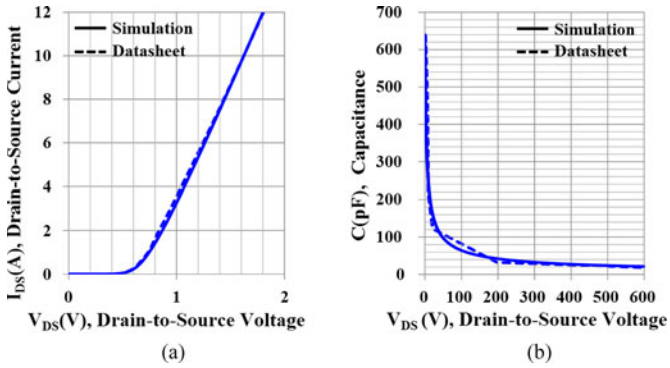

Fig. 5. GaN Schottky diode (a) *I–V* and (b) *C–V* characteristic.

TABLE II
ELECTRICAL SPECIFICATIONS OF THE CURRENT SHUNT

Part No.	Resistance	Bandwidth	P_{MAX}	E_{MAX}
SSDN-10	0.10 ohms	2000 MHz	2 W	2 J

parasitics as the test circuit to reveal the intrinsic switching performance of the device. Fig. 4(a) and (b) shows the DPT schematic and prototype, respectively. In the DPT, the 600-V cascode GaN HEMT is the device under test.

The free-wheeling diode is a 600-V GaN Schottky diode from Transphorm Inc., which almost eliminates the reverse-recovery effect, and thus, would not cause extra current overshoot and switching loss during the turn-on transition.

The GaN Schottky diode is also modeled in detail by Transphorm Inc., as shown in Fig. 5.

The device current is measured by a coaxial current shunt (part number SSDN-10) manufactured by T&M Research Products Inc., which has accurate resistance, small parasitic inductance, and high bandwidth. Table II shows the electrical characteristic

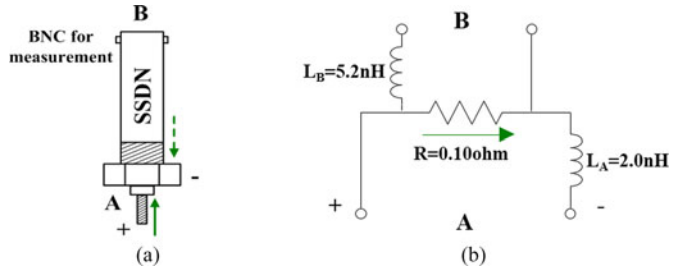

Fig. 6. Modeling of a coaxial current shunt: (a) prototype and (b) model.

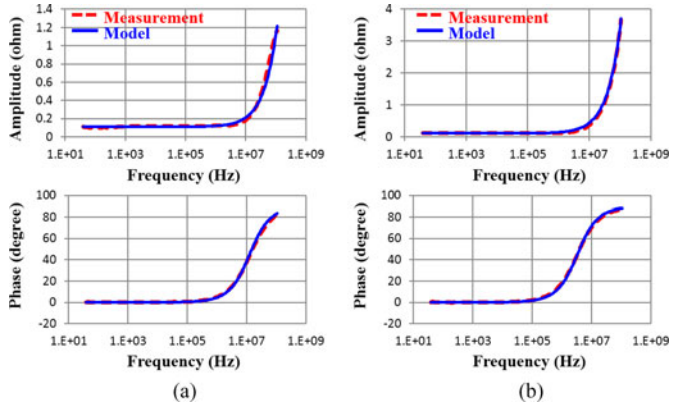

Fig. 7. Comparison of impedance from (a) terminal A and (b) terminal B between measurement and model.

specifications [24] of the current shunt. The operation principle of the current shunt is elaborated in [21]. Following the same modeling method discussed in [21], the current shunt is modeled by the circuit shown in Fig. 6. Both of the parasitic inductances are measured by an Agilent 4294A impedance analyzer with proper adaptors.

The model of the current shunt is verified by matching the impedance with the measurement results in impedance analyzer. Fig. 7 shows that the model matches well with measurement in terms of both magnitude and phase.

The printed circuit board (PCB) layout is optimized with minimized parasitic inductance, in which the commutation loop inductance is around 3.6 nH as extracted by Q3D FEA simulation. The low-side gate driver is driver IC ISL89163, which has strong driving capability; a 0-Ω gate resistor is used at the same time in order to turn ON and turn OFF the device as quickly as possible.

A series of double-pulse tests were conducted with the 400-V dc bus voltage, while the inductor current varied from 2 to 15 A.

B. Simulation Model Verification

The typical turn-on and turn-off waveforms are shown in Fig. 8. The waveforms indicate that the results of the simulation match well with the experiments, with the rising and falling slopes exactly matched, accurately predicted spikes, and similar oscillations are predicted with close magnitude and frequency. More severe spikes and oscillations are observed during the turn-on transition, when the junction capacitor of the free-wheeling diode is being charged.

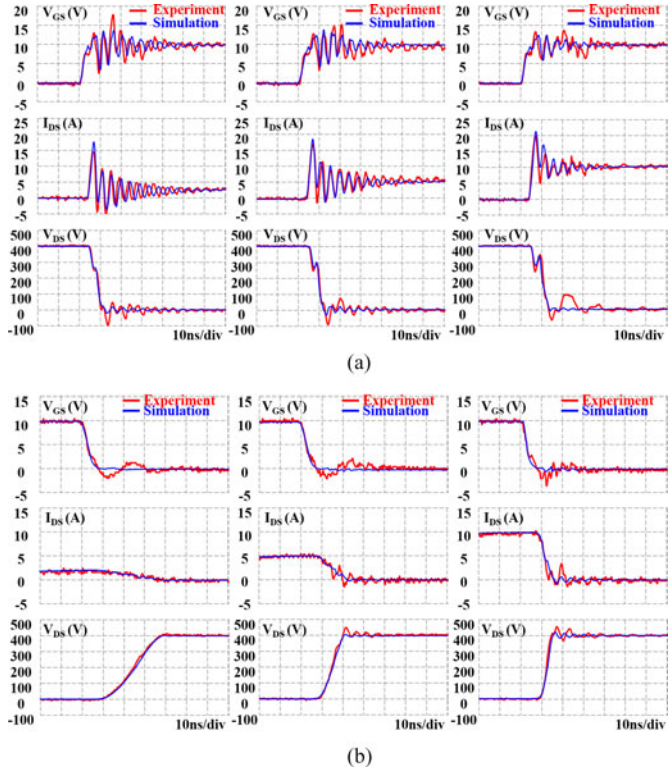

Fig. 8. GaN HEMT switching waveforms. (a) turn On at 400 V, 2 A/5 A/10 A; (b) turn OFF at 400 V, 2 A/5 A/10 A.

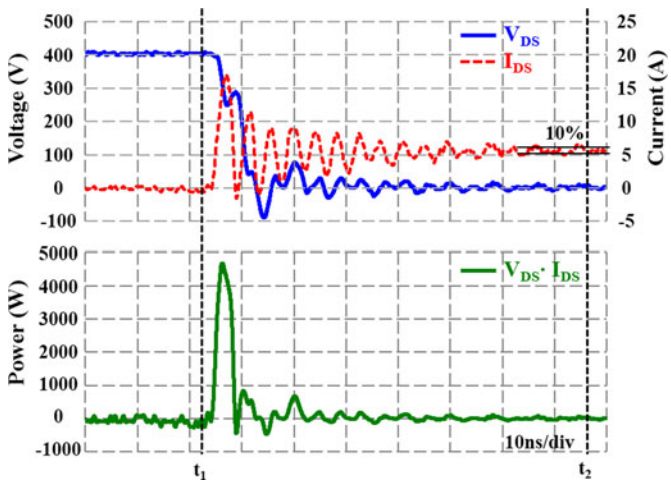

Fig. 9. Calculation of the turn-on energy.

Based on the switching waveforms, the switching energies can be defined and calculated. The turn-on energy $(E_{\rm ON})$ and turn-off energy $(E_{\rm OFF})$ are defined as the energies dissipated on the switch during the turn-on transition and turn-off transition. Fig. 9 shows the calculation of $E_{\rm ON}$ based on the experimental waveforms of $V_{\rm DS}$ and $I_{\rm DS}$. To be specific, the green curve is the product of $V_{\rm DS}$ and $I_{\rm DS}$ which is the instantaneous power dissipated on the device. Then, the integral of the instantaneous power from t_1 (the instant when $I_{\rm DS}$ starts to increase) to t_2 (the instant when $I_{\rm DS}$ settled to steady state within 10% error band) is defined as $E_{\rm ON}$. $E_{\rm OFF}$ is calculated following the same method. In this way, the calculated switching energy will contain

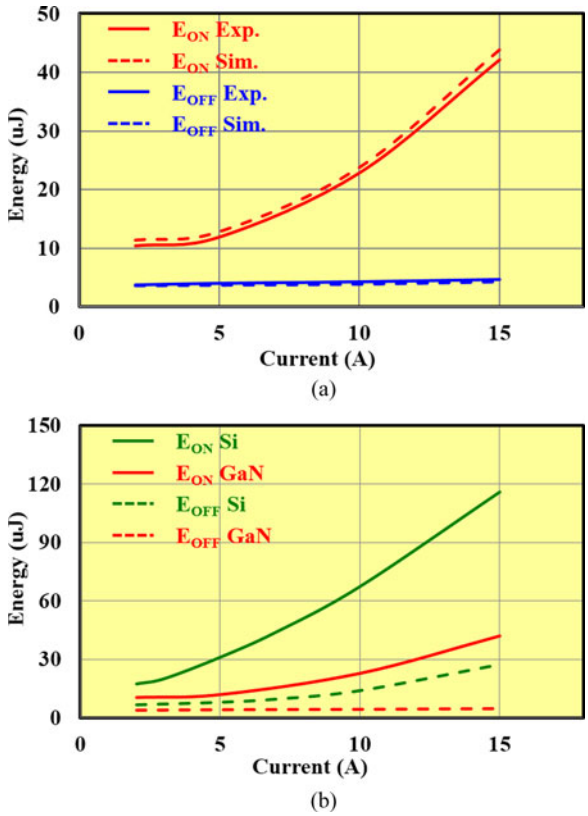

Fig. 10. Double-pulse test switching energy comparison. (a) Experiment and simulation results of GaN; (b) experiment results of GaN and Si.

not only the main transition loss, which is usually the major part of switching loss, but also the ringing loss, caused by parasitic oscillation and is not negligible in this case, during the entire switching transition.

The switching energies in different load currents are measured and shown in Fig. 10(a). The results of the simulation also match well with experiments. It is a clear trend that the turn-on energy is much larger than the turn-off energy, which is due to severe current spikes and oscillations, in all ranges of load currents. This phenomenon is also observed in the cascode SiC JFET [25]. In addition, the turn-on energy is a strong function of the load current. In contrast, the turn-off energy is extremely small and almost constant under different load currents. This phenomenon is unique and related to the distinctiveness of the cascode structure, which will be addressed in a future publication.

Compared to the state-of-the-art super junction Si MOSFET with similar voltage rating, current rating, and on resistance (part no. IPP60R160C6), the switching energy of the cascode GaN HEMT is significantly smaller as shown in Fig. 10(b). In addition, unlike the almost constant turn-off energy of GaN, the turn-off energy of Si MOSFET will increase with the turn-off current gradually.

It should be mentioned that the measurement and calculation of the turn-on energy and turn-off energy is taken from the terminal of the device. As a result, the energy stored in the output capacitor $(C_{\rm OSS})$ is counted during the turn-off transition, but this part of energy is actually dissipated during the turn-on

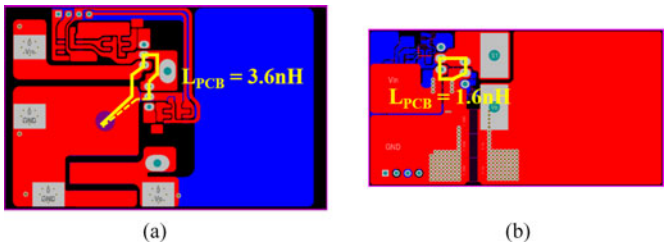

Fig. 11. Layout comparison between (a) DPT and (b) buck converter.

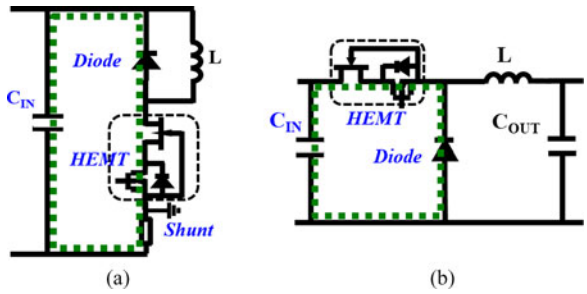

Fig. 12. Schematic comparison between (a) DPT and (b) buck converter.

TABLE III
PARASITIC INDUCTANCE COMPARISON

	DPT	Buck
L_{PCB}	3.6 nH	1.6 nH
$L_{Cin\_Package}$	0.3 nH	0.3 nH
$L_{HEMT\_Package}$	3.0 nH	3.0 nH
$L_{Diode\_Package}$	1.8 nH	1.8 nH
$L_{Shunt\_Package}$	2.0 nH	-
Loop	10.7 nH	6.7 nH

transition. To be specific, during the turn-on transition, the $C_{\rm OSS}$ is discharged through the channel of the device, which generates switching loss, but this discharging process cannot be observed from the measurement on device terminals. So it is a consensus [21] that in a double-pulse test, the turn-on energy is underestimated, and the turn-off energy is overestimated. The sum of $E_{\rm ON}$ and $E_{\rm OFF}$ is more meaningful when it is used to predict the switching loss.

C. Impact of the Current Shunt

In the double-pulse test, the measurement of current waveforms using a current shunt will introduce extra loop inductance. So it is a question that whether the double-pulse test can reflect the real switching loss distribution. In order to compare the impact of the current shunt in terms of switching loss measurement, a traditional buck converter is built for comparison. The buck converter uses the same devices as the DPT, while loop inductance introduced by the PCB can further be shrunk as the current shunt is removed. Figs. 11 and 12 show the comparison of the PCB and schematic, respectively. Table III shows the comparison of parasitic inductance on the commutation loop. More than 30% total commutation loop inductance is saved in an optimized buck converter design than an optimized DPT design.

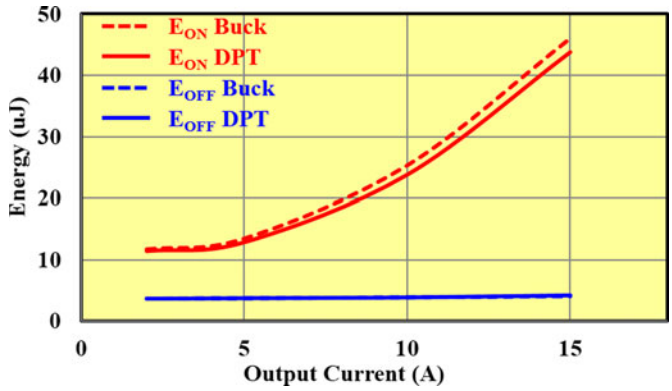

Fig. 13. Switching energy comparison between DPT and buck converter.

Circuit simulations are conducted for both the buck converter and the DPT, and corresponding switching loss distributions are compared (shown in Fig. 13). As the buck converter has smaller loop inductance, higher turn-on loss and lower turn-off loss are observed. This trend is in accordance with the conclusions in [21]. However, the differences are not significant. Through this comparison, it can be concluded that under careful design, a DPT can reflect the trend of real switching loss distribution in a bridge configuration converter with small differences.

IV. INVESTIGATION OF PACKAGE INFLUENCE

Due to the merits of the cascode GaN HEMT, the device is able to switch at very fast speed. However, as a result of the parasitics introduced by the bulky package, large switching losses and severe oscillations are observed during the switching transitions, which definitely limit the switching performance of the device, and cause potentially more electromagnetic interference for none-optimum circuit designs.

For the package influence study, many efforts are spent on the Si MOSFET with a single-switch structure [19], [26], [27]. It is common sense that the common-source inductance (CSI), which is defined as the inductance shared by power loop and driving loop, is the most critical parasitics. The CSI acts as negative feedback to slow down the driver during the turn-on and turn-off transitions, and thus, prolongs the voltage and current crossover time, and significantly increases the switching loss.

Recently, there have been some publications discussing the package influence for wide-bandgap devices, like the high-voltage SiC MOSFET and low-voltage GaN HEMT [5], [21]. The devices also use a single-switch structure, and therefore, the conclusions are similar to that of the Si MOSFET, which means the CSI still has major impact on the device's switching loss. However, due to the uniqueness of the cascode structure, the definition of the CSI is not straightforward. So far, there have been few papers that address this issue. In this paper, the analysis starts from the identification of critical parasitic inductance.

Following the same definition of CSI in a single-switch structure, the CSI of the low-voltage Si MOSFET and of the high-voltage GaN HEMT are analyzed. From the perspective of the Si MOSFET [see Fig. 14(a)], the blue loop is the power loop and the red loop is the driving loop. It is clear that $L_{\rm int3}$ and L_S are shared by the two loops, so they are the CSIs of the Si

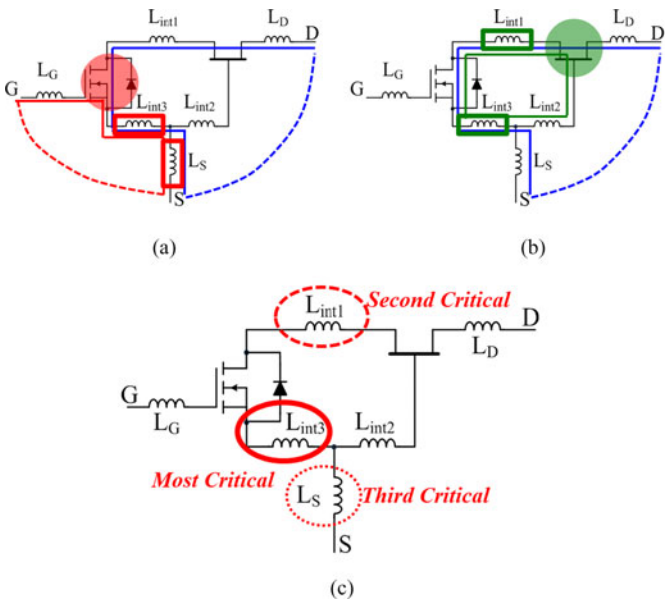

Fig. 14. Critical parasitic inductance analysis from the perspective of (a) Si MOSFET, (b) GaN HEMT, and (c) cascode structure.

MOSFET. Similarly, from the perspective of the GaN HEMT [see Fig. 14(b)], the blue loop is still the power loop, but the driving loop is changed to the green loop. As a result, $L_{\rm int3}$ and $L_{\rm int1}$ are the CSIs of the GaN HEMT.

Therefore, in terms of the cascode structure [see Fig. 14(c)], since $L_{\rm int3}$ is the CSI for both the GaN HEMT and the Si MOSFET, it should be the most critical parasitic inductance. $L_{\rm int1}$ is estimated to be the second-most critical inductance, since it is the CSI of the high-voltage GaN HEMT, which has the major switching loss. Last but not least, L_S is predicted to be the third-most critical inductance.

After theoretical analysis, the simulation model is used to verify the predictions. A circuit-level simulation is conducted based on a buck converter design working under the continuous-current-mode hard-switching condition. The switching loss during the hard-switching condition is the major concern for evaluation. Since the turn-on switching loss is the dominant part, the turn-on energy under 400 V/10 A conditions is chosen for comparison. A series of simulation waveforms is shown in Fig. 15, in which the simulation results based on the TO-220 package is always set as the benchmark (red line), while each comparison case (blue line) removes one of the six parasitic inductance to evaluate the impact of that specific parasitic inductance.

By comparing waveforms, the different impacts of each parasitic inductance can be observed. Without L_D or $L_{\rm int2}$, the waveforms have almost no difference; without L_G, there is an obvious forward phase shift for $I_{\rm DS}$ and $V_{\rm DS}$; however, in terms of the turn-on energy, there is still no significant difference. In contrast, when without L_S, $L_{\rm int1}$ or $L_{\rm int3}$, the $I_{\rm DS}$ has higher overshoot, while the $V_{\rm DS}$ has sharper falling edge compared to the benchmark; thus shorter crossover times and smaller turn-on energies are observed in these three cases.

For better quantitative comparison, the simulated turn-on switching loss is shown in Fig. 16. Based on the TO-220 package case, the total turn-on energy is 23.6 μJ under 400 V/10 A condition, which is set as the benchmark. By eliminating the impact of L_D, $L_{\rm int2}$, or L_G, the reduction of turn-on switching loss is negligible (around 1% of 23.6 μJ). On the other hand, when the critical parasitic inductance like L_S, $L_{\rm int1}$, or $L_{\rm int3}$ is removed, the turn-on switching loss will reduce significantly (9%, 15%, and 22% of 23.6 μJ, respectively).

In summary, the simulation results have quantitatively justified the predictions of the theoretical analysis, that the $L_{\rm int3}$, $L_{\rm int1}$ and L_S are identified to be the most critical package parasitic inductance. For future research regarding packaging improvement, these three inductances should be minimized in priority. Furthermore, it could be project that if an advanced package realized, which is able to eliminate all three critical parasitic inductances, the total device switching loss should have a significant reduction, while better switching performance is expected.

V. Loss Analysis Based on the Buck Converter

After the development and verification of the simulation model, it can be used as a tool to analyze the switching performance of a given power converter. For the application of bidirectional battery charger/discharger, a 380 V/200 V bidirectional buck–boost converter is built with 600-V cascode GaN HEMTs as both the top switch (TS) and the bottom switch (BS) (see Fig. 17). For TS driving, the ICs NCP5181 and ISL89163 are used in series; for BS driving, only the ISL89163 is used. The PCB is also carefully designed with minimized parasitic inductance of 1.6 nH for the commutation loop and 3.3 nH for the TS/BS driving loop.

Fixed frequency continuous-current-mode (CCM) is used for the hard-switching; the inductor peak–peak current ripple is 3 A, which is 50% of the full-load current. While variable-frequency critical mode (CRM) is used for soft-switching demonstration; the CRM could achieve both zero voltage switching (ZVS) turn ON of TS and ZCS turn OFF of BS; the inductor peak–peak current ripple is more than twice the load current under any load conditions. The efficiency curves shown in Fig. 18(a) reveals a clear trend that soft switching is superior to hard switching in all load ranges tested.

Furthermore, a converter loss breakdown is conducted and shown in Fig. 18(b), in which the total inductor loss, including core loss and winding loss, are tested according to the methods proposed in [28]; the conduction loss and the switching loss are calculated by the developed simulation model.

Under hard-switching conditions, the TS turn-on loss is the dominant part of total loss. Fig. 19 shows the corresponding TS turn-on waveforms. Even though the load current is only around 5 A, the current overshoot reaches 25 A peak value. This is due to the reverse-recovery effect and junction capacitor charging of the BS (highlighted by the red area). The crossover between the high-voltage and high-current overshoots results in a large turn-on loss. It can also be observed that the di/dt is about 3000 A/μs, which is much higher than the traditional 600-V Si MOSFET. This high speed is due to the inherent characteristics of the GaN HEMT.

When comparing hard switching with soft switching, the loss breakdown indicates that the TS turn-on loss is the dominant loss

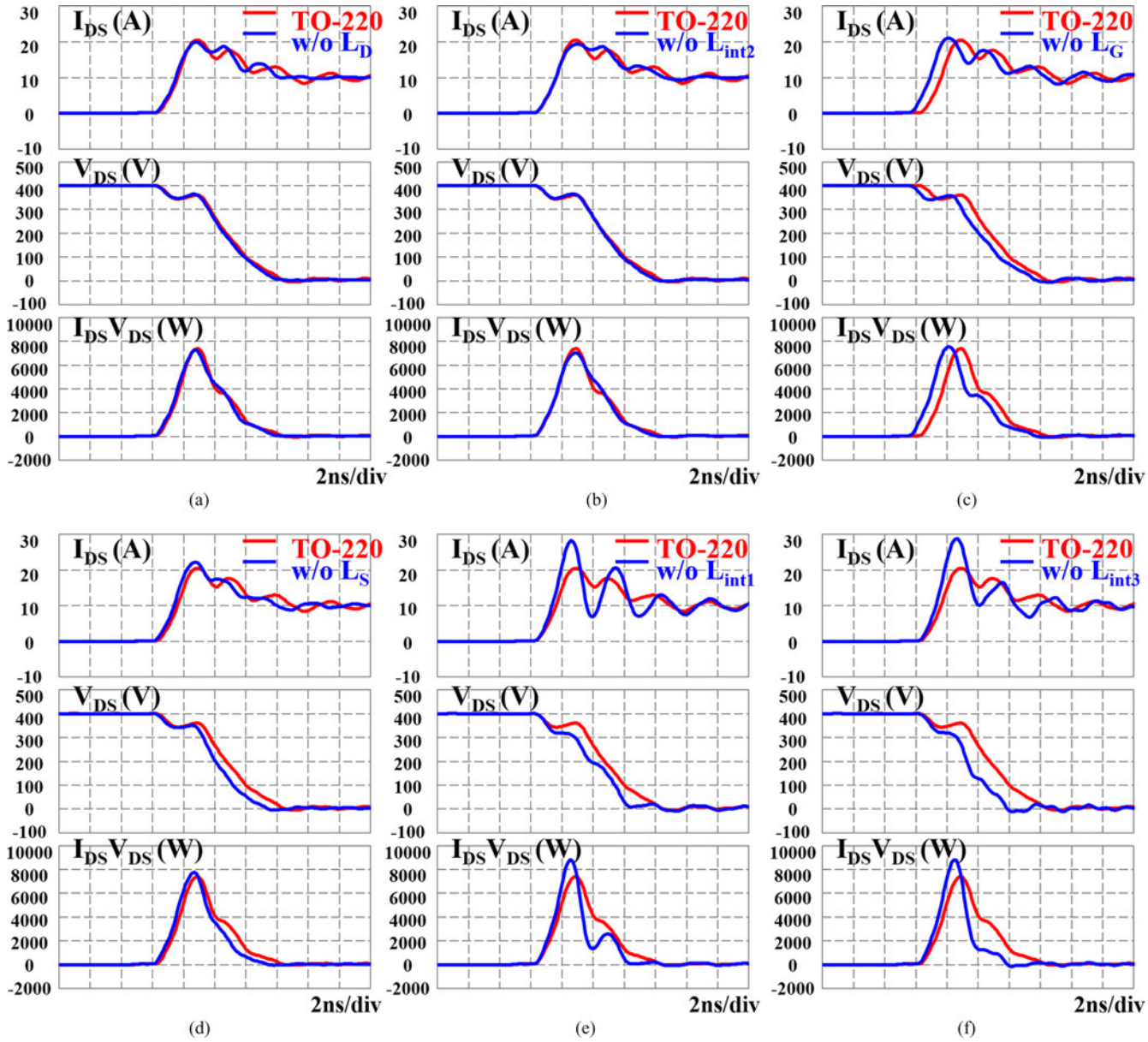

Fig. 15. Top switch hard-switching turn-on waveforms comparison under 400 V/10 A condition. The impacts of parasitic inductance (a) L_D, (b) L_{int2}, (c) L_G, (d) L_S, (e) L_{int1}, and (f) L_{int3}.

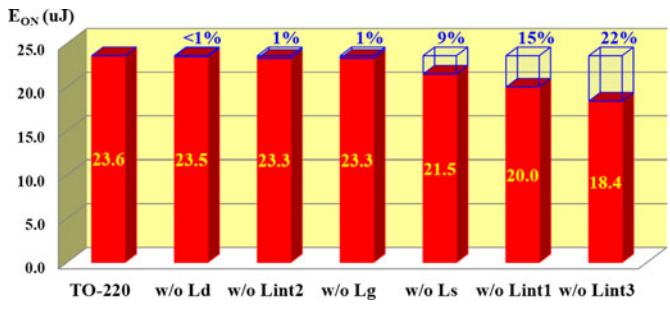

Fig. 16. Top switch turn-on energy comparison under 400 V/10 A condition.

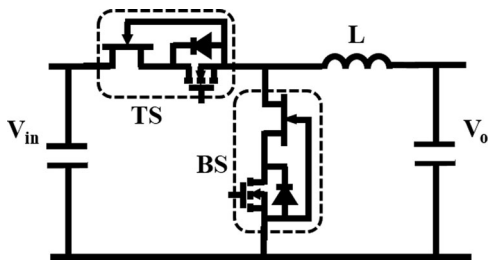

Fig. 17. Bi-directional buck–boost converter schematic.

under hard-switching conditions, much larger than any other loss; this is why hard switching has much lower efficiency. In the soft-switching case, due to higher turn-off current and RMS current, the price paid is a little bit higher conduction loss, turn-off loss and inductor loss, while turn-on loss is eliminated as a tradeoff. In total, soft switching gains a lot in terms of efficiency.

If still comparing GaN with the state-of-the-art Si MOSFET for CCM hard-switching condition, the reverse recovery of the body diode of high voltage Si MOSFET will lead to tremendous

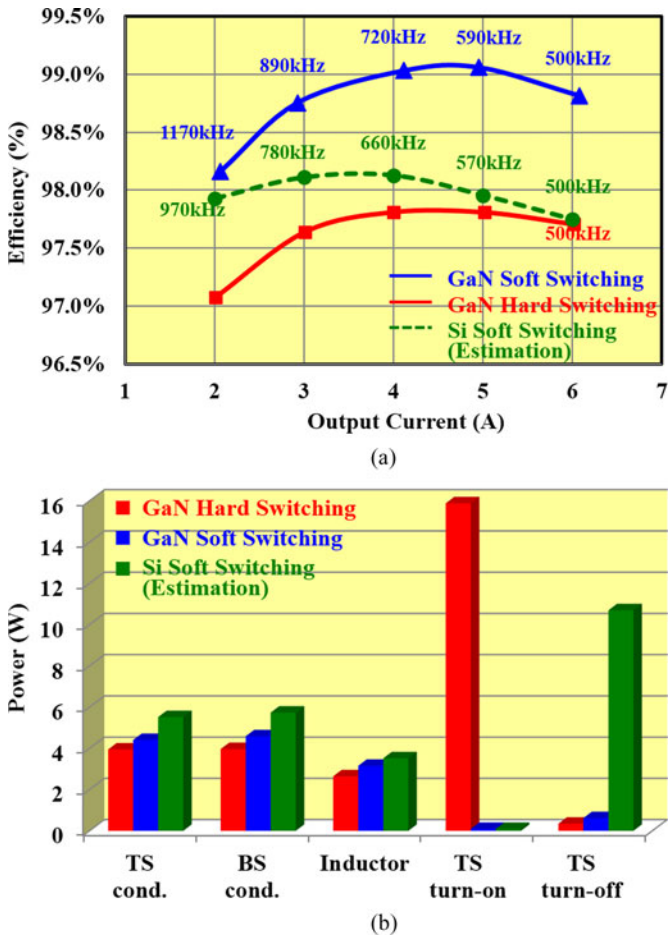

Fig. 18. Comparison between hard switching and soft switching. (a) Buck converter efficiency; (b) loss breakdown under 6 A condition.

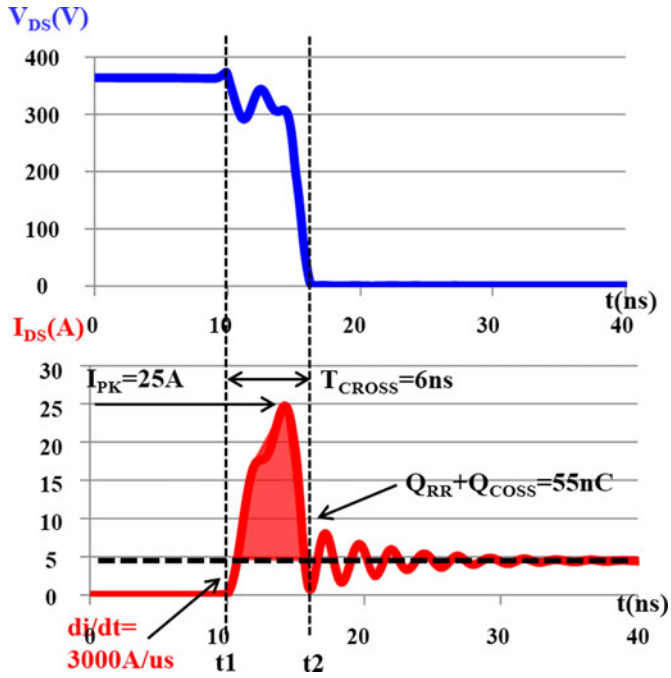

Fig. 19. Buck converter top switch turn-on waveforms (simulation) under CCM hard-switching condition.

turn-on loss, so the switching frequency can hardly be pushed to 500 kHz; for CRM soft-switching condition, an estimation of efficiency and loss breakdown are also included in Fig. 18. The major difference is Si MOSFET has large turn-off loss, which is also increased with the turn-off current, so the efficiency will drop significantly under the full-load condition. Furthermore, since the output capacitance of Si is about four times of GaN, there will be longer resonant time to achieve ZVS. This will result in more duty cycle loss for energy transfer and higher conduction loss.

In summary, these experiments indicate that the characteristics of the cascode GaN HEMT are superior to the state-of-the-art Si MOSFET, and soft switching is still critical for the device to achieve expected high-efficiency operation in the megahertz high-frequency range.

VI. Conclusion

The accurate extraction of package parasitic inductance is an important step in building a practical device simulation model. According to different device working conditions, the current direction of each conductor needs to be clearly defined before FEA simulation. Different parasitic inductances for the turn-on and turn-off transitions are required when conducting circuit-level simulation. The accuracy of the simulation model is verified by experiments under different working conditions. Based on the simulation model, the influence of the device package is discussed, including the uniqueness of the cascode structure. Several critical parasitic inductances are identified through theoretical analysis, and verified by the simulation model, which provides a strong theoretical support for continuing packaging optimization research. Finally, a detailed buck converter loss breakdown is made, and both experiment and simulation indicate that soft-switching is the most promising operation mode to continue to raise the switching frequency in megahertz range and maintain high efficiency, which is probably the best way to fully utilize the advantages of the high-voltage GaN HEMT for the future power conversion technology.

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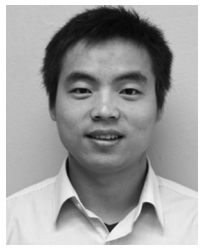

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